


PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) NVDA/P000455	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed Name _____		Application Number 10/804,945 First Named Inventor Curtis R. PRIEM Art Unit 2111	Filed March 19, 2004 Examiner Thomas J. Cleary
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>			
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> attorney or agent of record. Registration number 52,371 <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number _____		<div style="text-align: center;">  Signature </div> <hr/> <div style="text-align: center;"> Stephanie Winner Typed or printed name </div> <hr/> <div style="text-align: center;"> 713-623-4844 Telephone number </div> <hr/> <div style="text-align: center;"> June 6, 2008 Date </div> <hr/>	
<input checked="" type="checkbox"/> *Total of 1 forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
Curtis R. PRIEM	§	Confirmation No.: 9182
	§	
Serial No.: 10/804,945	§	Group Art Unit: 2111
	§	
Filed: March 19, 2004	§	Examiner: Thomas J. Cleary
	§	
For: METHOD AND	§	
APPARATUS FOR	§	
LATENCY BASED	§	
THREAD SCHEDULING	§	

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL CONFERENCE BRIEF

Dear Sir:

In conjunction with the Pre-Appeal Brief Request for Review filed herewith, Applicant requests a Panel review of the Final Rejection in this matter (see the Final Office Action dated March 6, 2008). Although the remarks herein are focused on a specific factual issue raised by the rejection, nothing in this paper is meant to limit the scope of any arguments, either factual or legal, that Applicant may later present in a full appeal brief.

QUESTIONS FOR REVIEW

The Examiner has rejected pending claims 1, 3-6, 9-10, and 23 under 35 U.S.C. 103(a) as being unpatentable over Zolnowsky (U.S. Patent No. 5,826,081), Browning (U.S. Patent No. 6,633,897), and Jones (U.S. Patent No. 5,812,844). The Examiner also rejected claims 1-15, 17-18, and 23 under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan (U.S. Patent No. 6,085,215), Jones, and Browning. The Examiner's rejections are respectfully traversed. Specifically, Applicants disagree with the Examiner's position that the combination of Zolnowsky, Browning, Jones, and Ramakrishnan teach or suggest the limitations of (i) masking interrupts, (ii) unmasking

interrupts), (iii) simultaneously rearranging threads in a single queue, and (iv) ordering all requests from the hardware devices in the single queue.

ARGUMENTS SUBMITTED

Claims 1 and 9 recite the limitations of (i) masking interrupts from hardware devices, (ii) unmasking interrupts from the hardware devices, (iii) simultaneously rearranging threads in a single queue, and (iv) ordering all requests from the hardware devices in the single queue. The single queue represents the order in which all threads will be serviced for all of the hardware devices. Zolnowsky, Jones, Browning, and Ramakrishnan fail to teach or suggest these limitations.

In contrast to the claimed approach, Zolnowsky teaches using several queues instead of a single queue. Consequently, all of the requests are not ordered in a single queue, as recited in claims 1 and 9. In particular, each one of the processors disclosed in Zolnowsky has a dedicated queue, and a global dispatch (real time) queue is used for higher priority real time threads. Multiple schedulers select threads for processing from any of the queues. Therefore, the order in which the threads will be serviced is determined by the multiple schedulers rather than the order in which the threads are arranged any of the queues (see Figure 7, col. 8, lines 19-38). However, Zolnowsky also fails to teach or suggest the limitations of masking and unmasking interrupts from hardware devices. The Examiner states that the limitations of masking and unmasking interrupts are described in col. 6, lines 34-42 of Zolnowsky where scheduling locks are described. Zolnowsky teaches that each queue has a lock that must be acquired by a scheduler in order to dispatch a thread from the queue. The per-queue lock is needed since any scheduler can access any queue. Nowhere does Zolnowsky suggest that a lock is used to mask or unmask interrupts. With regard to interrupts, Zolnowsky teaches that "interrupt threads are always given the highest priority" (see col. 8, lines 3-4). Nowhere does Zolnowsky teach or suggest that interrupts are masked or unmasked, as recited in claims 1 and 9.

Jones also fails to teach or suggest the limitations recited in claims 1 and 9 set forth above. Jones teaches the scheduling of interrupts and other processing tasks. Nowhere does Jones teach or suggest that interrupts are masked or unmasked. Jones

only describes using an interrupt queue and several "lists" of threads. Further, nowhere does Jones teach or suggest ordering all requests from the hardware devices in the single queue. As shown in Figure 6A of the reference, a processor list, ready list, and blocked list are each maintained for scheduling purposes. Thus, Jones fails to teach or suggest simultaneously rearranging the order in which all threads will be serviced from a single queue. All of the requests are not ordered in a single queue, as recited in claims 1 and 9.

Like Zolnowsky and Jones, Browning also fails to teach or suggest the limitations recited in claims 1 and 9 set forth above. In particular, Browning does not teach or suggest that interrupts are masked or unmasked. Browning also fails to teach or suggest ordering all requests from the hardware devices in the single queue. In column 5, lines 8-11, Browning describes the preferred embodiment of the global queue as being "subdivided into 128 first-in-first-out (FIFO) queues, where there is a unique queue for each priority level." Rather than being a single queue, the global queue is actually made up of multiple queues, with a different queue for each priority level. The statement in col. 6, lines 1-3 that "it will be understood by those skilled in the art that various changed in form and detail may be made therein without departing from the spirit and scope of the invention" does not rise to the level of a teaching or suggestion of a single queue.

Additionally, Browning does not teach or suggest that the threads are simultaneously rearranged in the single queue in an order in which the threads will be serviced. Instead of rearranging the order of the threads in the single queue, the dispatcher taught by Browning selects a thread for processing from a run queue that is subdivided into multiple FIFO queues (see col. 5, lines 8-10). Therefore, the order in which the threads will be serviced is determined by the dispatcher rather than the order in which the threads are arranged in a single queue.

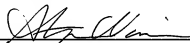
Ramakrishnan also fails to teach or suggest the limitations recited in claims 1 and 9 set forth above. Ramakrishnan teaches performing minimal interrupt processing. Nowhere does Ramakrishnan teach or suggest that interrupts are masked or unmasked as recited in claims 1 and 9. Further, Ramakrishnan also fails to teach or suggest ordering all requests from the hardware devices in the single queue. Ramakrishnan

teaches using a round-robin scheduler to select each thread for execution from a real time domain and a general purpose domain. The order in which the threads will be serviced is determined by the round-robin scheduler rather than the order in which the threads are arranged in a single queue. Nowhere does Ramakrishnan teach or suggest that threads are simultaneously rearranged in a single queue in an order in which the threads will be serviced.

The other references cited by the Examiner fail to cure the deficiencies of Zolnowsky, Browning, Ramakrishnan, and Jones relative to claims 1 and 9. Therefore, no combination of the cited references can render either claim 1 or claim 9 obvious. Since claims 2-8, 17-18, and 21-23 depend from claim 1 and claims 10-15 depend from claim 9, no combination of the cited references can render these claims obvious.

All of the claims currently pending in the application are therefore patentable over Hayes. In view of these clear distinctions, reconsideration and allowance of all the claims is respectfully requested.

Respectfully submitted,



Stephanie Winner
Registration No. 52,371
PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (650) 330-2310
Facsimile: (650) 330-2314
Agent for Applicant